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12-23-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO. 088941/0184

Applicant: Atsushi YOSHIKAWA et al.

Title: DELAY ADJUSTMENT CIRCUIT AND A CLOCK GENERATING CIRCUIT USING THE SAME

Appl. No.: Unassigned

Filing Date: 02/02/2001

Examiner: Unassigned

Art Unit: Unassigned

09775956.020201

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the present Application, Applicants respectfully request that the above-identified application be amended as follows:

IN THE CLAIMS:

Claim 4, line 2, delete "any of claims 1" and insert --claim 1--;
line 5, delete "one or more of Claims 1 through 3" and insert --claim 1--.

Claim 6, line 2, delete "any of Claim 1 through Claim 3" and insert --claim 1--;
line 5, delete "any of Claims 1 through 3" and insert --claim 1--.

Please add the following new claims:

--12. A clock generating circuit comprising:

the delay adjustment circuit according to claim 2 into which a reference clock is input; and